Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A high-speed router for transmitting data packets[[,]] containing header data and useful data[[,]] between data networks, the router comprising:

a plurality of data-processing processors for parallel data processing of the header data;

a demultiplexer for separating the data packets into header data and useful data; and

a distribution processor for distributing the [~~separated~~] header data among the data[-]processing processors[~~, wherein the distribution processor distributes the header data~~] at least in part on the basis of a priority specified by the header data and [[~~the~~]] a workload of the data-processing processors.

2.-4. (Canceled)

5. (Currently Amended) The high-speed router as claimed in claim 1, wherein the distribution processor is configured to distribute the header data among the data-processing processors by means of DMA operations.

6. (Previously Presented) The high-speed router as claimed in claim 1, further comprising a CAM coprocessor having an associative memory for classifying the data packets.

7. (Previously Presented) The high-speed router as claimed in claim 1, further comprising a useful-data memory for buffer-storing the separated useful data.

8. (Previously Presented) The high-speed router as claimed in claim 1, wherein header data and useful data corresponding to a data packet each have a respective identifier associated with the corresponding data packet.

9. (Currently Amended) The high-speed router as claimed in claim 7, further comprising a first multiplexer for compiling header data and useful data into data packets, the first multiplexer being configured to accept useful data from at least one of the useful-data memory [~~or from~~] and a switching mechanism.

10. (Currently Amended) The high-speed router as claimed in claim 9, further comprising a second multiplexer for compiling the [~~useful data~~] buffer-stored separated useful data in the useful data memory and the header data.

11. (Previously Presented) The high-speed router as claimed in claim 9, further comprising a FIFO memory connected downstream of the first multiplexer for outputting the compiled data packets through the router.

12. (Previously Presented) The high-speed router as claimed in claim 10, wherein the output of the second multiplexer is connected to the switching mechanism.

13. (Currently Amended) The high-speed router as claimed in claim 6, wherein the distribution processor, the data-processing processors and the CAM coprocessor are connected to a common header-data bus.

14. (Currently Amended) The high-speed router as claimed in claim 1, wherein each data-processing processor is connected to a respective dedicated local memory.

15. (Currently Amended) The high-speed router as claimed in claim 13, further comprising a common memory connected to the header-data bus.

16. (Currently Amended) The high-speed router as claimed in claim 13, wherein the CAM coprocessor is connected to the header-data bus via FIFO buffer memories.

17. (Previously Presented) The high-speed router as claimed in claim 1, further comprising an input buffer connected upstream of the demultiplexer.

18. (Previously Presented) The high-speed router as claimed in claim 1, configured to transmit data packets between a first data network and a second data network, the first data network comprising a LAN network.

19. (Previously Presented) The high-speed router as claimed in claim 1, configured to transmit data packets between a first data network and a second data network, the second data network comprising the Internet.

20. (Currently Amended) The high-speed router as claimed in claim 1, wherein the distribution processor and the data-processing processors are processors of the same processor type.

21. (New) A system comprising

a first data network; and

a high-speed router as recited in claim 1, the high-speed router being configured to transmit data packets between the first data network and a second data network.